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EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/538,369	BURNS ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6,8,13,15-18 and 20-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6,8,13,15-18 and 20-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 4-6, 8, 13, 15-18, and 20-25 are pending.

2. The office acknowledges the following papers:

Claims and arguments filed on 4/2/2009.

New Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 5-6, 8, 13, 15-16, and 21-24 are rejected under 35 U.S.C. §103(a) as being unpatentable over Higuchi et al. (U.S. 5,822,605).

5. As per claim 1:

Higuchi disclosed a coprocessor coupled to a main processor having an execution speed greater than that of said coprocessor (Higuchi: Figure 1 elements 100 and 140, column 8 lines 33-50)(Element 140 is the main processor and all of the processing element (100) combined make up the coprocessor. It's obvious to one of ordinary skill in the art that the coprocessor is faster executing instructions than the host processor.), the coprocessor comprising:

a two-dimensional array of processing cells, including a plurality of periphery cells located on peripheral sides of the array (Higuchi: Figure 1 element

100)(Processing elements PE 11-12 and PE 21-22 make up the two-dimensional array, where each element is a peripheral cell.); and

an interface module surrounding the two-dimensional array of processing cells (Higuchi: Figure 1 elements 116 and 132-139)(The exchange switches (minus EX 11-12 and EX 21-22) and the XB buses make up the interface module.), comprising:

a plurality of input/output (I/O) pads for the coprocessor (Higuchi: Figure 3 elements 30-32, column 14 lines 11-15)(Element 30 is an output pad for the processing element and elements 31-32 are input pads for the processing element. There are pluralities of these elements because elements 30-32 are replicated for each processing element.),

a plurality of border cells disposed along an outside of the two-dimensional array and surrounding the two-dimensional array, each border cell being connected to a corresponding one of the periphery cells, each border cell including a buffer connected to the corresponding one of the periphery cells (Higuchi: Figure 3 elements 303 and 304, column 15 lines 8-16)(The output ports sending data to the crossbar buses buffers data being indirectly input to a processing element. For example, output port 303 in EX 20 is indirectly connected to PE 21 via XB-X2 and EX 21. Thus, the output ports of the surrounding exchanges are connected to each of the periphery cells of the processing array.), and

a crossbar network for reconfigurably connecting each of the I/O pads to a selectable one of the border cells (Higuchi: Figures 1 and 3 elements 132-139 and 310, column 8 lines 33-40 and column 15 lines 1-7),

wherein the buffer of each border cell connects to the corresponding one of the periphery cells (Higuchi: Figure 3 elements 303 and 304, column 15 lines 8-16)(The output ports sending data to the crossbar buses connects indirectly to a processing element. For example, output port 303 in EX 20 is indirectly connected to PE 21 via XB-X2 and EX 21.) and connects through the crossbar network to the I/O pad connected to the border cell (Higuchi: Figures 1 and 3 elements 30-32, 116, 132-139, and 303-304)(The border cells 303-304 connects to the I/O pads 30-32 in other exchanges through the crossbar buses 132-139.)

6. As per claim 5:

Higuchi disclosed the coprocessor of claim 1, wherein the processing cells within the array are arranged in rows and columns such that one processing cell is interconnected to other of said processing cells such that said one processing cell is connected only to processing cells whose column is the same and whose row is immediately adjacent, and only to processing cells whose row is the same and whose column is immediately adjacent (Higuchi: Figures 1 and 3 elements 132-139 and 310, column 8 lines 33-40 and column 15 lines 1-7)(The limitation allows for a cell to connect to any other cell in its same row and column. The limitation also allows for connecting to cells in a row/column immediately adjacent. For example, processing element 11 in

the array connects to elements in the same row/column of processing element 11. Thus, reading on the claimed limitation.).

7. As per claim 6:

Higuchi disclosed the coprocessor of claim 1, wherein the coprocessor interface module and main processor of claim 1 and a shared memory that communicatively connects with the interface module and the main processor to provide the main processor to coprocessor connection (Higuchi: Figure 1 elements 100 and 140, column 8 lines 33-50)(Official notice is given that the host processor and coprocessor 2-D array can have a shared memory among themselves to store data. Thus, it's obvious to one of ordinary skill in the art that the host processor and coprocessor share a memory.).

8. As per claim 8:

Higuchi disclosed the coprocessor of claim 1, wherein said two-dimensional array of processing cells, said a plurality of periphery cells located on peripheral side of the array and said interface module are formed within an integrated circuit (Higuchi: Figure 1 element 100)(It's obvious to one of ordinary skill in the art that the system is implemented on an integrated circuit.).

9. As per claim 13:

Higuchi disclosed a functional unit comprising:

a main processor (Higuchi: Figure 1 element 140, column 8 lines 33-50)

a two-dimensional array of processing cells coupled to the main processor (Higuchi: Figure 1 elements 100 and 140, column 8 lines 33-50)(Element 140 is the main processor and all of the processing element (100) combined make up the

coprocessor.), the processing cells comprising non-periphery cells and periphery cells surrounding the non-periphery cells (Higuchi: Figure 1 element 100)(The inner 4 processing elements are the non-periphery cells surrounded by the outer 12 processing elements.),

a mechanism external to the two-dimensional array for reconfiguring a plurality of intra-processor information paths to the array to respective said periphery cells only (Higuchi: Figure 1 elements 132, 135-136, and 139 and figures 5-6 elements 504-507 and 705, column 15 lines 54-61 and column 16 lines 31-54)(The crossbar control is external to the 2-D array and there are four crossbars (elements 132, 135-136, and 139) they are contained in that only service periphery cells. These crossbars reconfigure the message paths through controlling the switches connecting processing elements.).

10. As per claim 15:

The additional limitation(s) of claim 15 basically recite the additional limitation(s) of claim 5. Therefore, claim 15 is rejected for the same reason(s) as claim 5.

11. As per claim 16:

Higuchi disclosed the unit of claim 13, further including means for transmitting a plurality of array programs to corresponding predetermined subsets of said processing cells (Higuchi: Figure 1 elements 116 and 132-139)(The exchange and crossbar elements are able to transmit data to the processing elements.).

12. As per claim 21:

Higuchi disclosed the coprocessor of claim 1, wherein said configuring the coprocessor configures the array in a is rectangular arrangement (Higuchi: Figure 1

elements 100)(The array of processing elements is square. However, it's obvious to one of ordinary skill in the art that the array can be expanded in size to result in a rectangular shape. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.), wherein the periphery consists of those of said processing cells located in all of a first row, last row, first column and last column of said array (Periphery by definition is the boundary of an area (The American Heritage Dictionary of the English Language, Fourth Edition), therefore the periphery of the array is inherently the first row, last row, first column and last column.), and wherein the interface module's mechanism for reconfiguring a plurality of information paths reconfigures information paths directly connecting the interface module and each of the cells on the periphery of the array (Higuchi: Figures 1 and 3 elements 132-139 and 310, column 8 lines 33-40 and 15 lines 1-7)(The crossbar network allows for reconfiguring paths within the 2-D array.).

13. As per claim 22:

Higuchi disclosed the coprocessor of claim 1, wherein the interface comprises a plurality of border cells directly connected to the respective processing cells on the periphery of the array (Higuchi: Figure 3 element 305, column 15 lines 8-16)(Output port buffers data being input to a processing element.).

14. As per claim 23:

Higuchi disclosed the coprocessor of claim 1, further comprising a master cell for forwarding array programs to the processing cells of the two-dimensional array (Higuchi:

Figure 1 element 140, column 8 lines 44-50)(The host processor is the master cell that loads programs to the 2-D array.).

15. As per claim 24:

The additional limitation(s) of claim 24 basically recite the additional limitation(s) of claim 1. Therefore, claim 24 is rejected for the same reason(s) as claim 1.

16. Claim 2 is rejected under 35 U.S.C. §103(a) as being unpatentable over Higuchi et al. (U.S. 5,822,605), further in view of Miyamori et al. ("REMARC: Reconfigurable multimedia array coprocessor").

17. As per claim 2:

Higuchi disclosed the coprocessor of claim 1.

Higuchi failed to teach the array comprises a systolic processing array.

However, Miyamori discloses the array comprises a systolic processing array (Miyamori: Figure 2, page 396 column 1 paragraph 2).

The advantage of arranging a reconfigurable architecture in a systolic manner is that it can exploit fine-grained parallelism and achieve higher performance versus other multimedia extensions (Miyamori: Page 389 column 2 paragraph 2). One of ordinary skill in the art would have been motivated by this advantage to allow for systolic processing on the processing array of Higuchi. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement systolic processing on the array of Higuchi to gain increased performance by exploiting fine-grained parallelism.

18. Claims 4 and 17-18 are rejected under 35 U.S.C. §103(a) as being unpatentable Higuchi et al. (U.S. 5,822,605), further in view of Barat et al. ("Reconfigurable instruction set processor: An implementation platform for interactive multimedia applications").

19. As per claim 4:

Higuchi disclosed the coprocessor of claim 1, wherein each processing cell of a plurality of the processing cells is connected by a respective plurality of four paths to corresponding four of said processing cells (Higuchi: Figure 1 element 100)(The processing elements can connect to four processing cells via four paths through the exchanges and crossbar buses.).

Higuchi failed to teach wherein the coprocessor is capable of performing mathematical operations having a timing based on a flow of input operands along the paths.

However, Barat disclosed wherein the coprocessor is capable of performing mathematical operations having a timing based on a flow of input operands along the paths (Barat: Page 484 column 1 paragraph 2)(The compiler generates code with timing delays of the processing elements and interconnects in mind. Official notice is given that instructions executed on a processor can include mathematical operations that use operands. Thus, it's obvious to one of ordinary skill in the art that the instructions executed are mathematical operations that use operands.).

The advantage of the reconfiguration method of Barat is that it allows for a compiler to more efficiently execute loops by storing configurations locally (Barat: Page

483, section 2.2 paragraph 2). One of ordinary skill in the art would have been motivated by this advantage to implement it within the processor of Higuchi. Thus, one of ordinary skill in the art at the time of the invention would have implemented the reconfiguration method of Barat into the processor of Higuchi for the advantage of more efficiently executing loops.

20. As per claim 17:

Higuchi disclosed a system including the functional unit of claim 16.

Higuchi failed to teach an array program generator for generating the array programs to be transmitted, and, when needed, updating a program, transmitting the updated program, and transmitting concurrently, when needed, a reconfigure signal to said mechanism to correspondingly update a current steady state connection pattern of said information paths.

However, Barat disclosed an array program generator for generating the array programs to be transmitted (Barat: Page 483, section 2.2 paragraph 2)(The compiler generates programs executed on the array of Higuchi.), and, when needed, updating a program, transmitting the updated program, and transmitting concurrently, when needed, a reconfigure signal to said mechanism to correspondingly update a current steady state connection pattern of said information paths (Barat: Page 483, section 2.2 paragraph 1)(The ROP field will be a signal to update the reconfigurable microcomputer clusters of Higuchi to be able to execute an instruction. The instruction that is executed is also transferred to the array to be executed.).

The advantage of the reconfiguration method of Barat is that it allows for a compiler to more efficiently execute loops by storing configurations locally (Barat: Page 483, section 2.2 paragraph 2). One of ordinary skill in the art would have been motivated by this advantage to implement it within the processor of Higuchi. Thus, one of ordinary skill in the art at the time of the invention would have implemented the reconfiguration method of Barat into the processor of Higuchi for the advantage of more efficiently executing loops.

21. As per claim 18:

Higuchi and Barat disclosed the system of claim 17, further including a compiler configured for receiving, in response to said program updating data representative of input and output timing for said unit (timing delay) and further configured for compiling an instruction based on said data (Barat: Page 484 column 1 paragraph 2)(The compiler generates code with timing delays of the processing elements and interconnects in mind.).

22. Claims 20 and 25 are rejected under 35 U.S.C. §103(a) as being unpatentable over Higuchi et al. (U.S. 6,434,689), in view of Cloutier (U.S. 5,892,962.).

23. As per claim 20:

Higuchi disclosed a method for interfacing a coprocessor to a main processor, comprising the steps of:

configuring the coprocessor to compromise a two-dimensional array of processing cells (Higuchi: Figure 1 element 100) and to have an execution speed

greater than that of said processor (Higuchi: Figure 1 elements 100 and 140, column 8 lines 33-50)(Element 140 is the main processor and all of the processing element (100) combined make up the coprocessor. It's obvious to one of ordinary skill in the art that the coprocessor is faster executing instructions than the host processor.), the processing cells comprising non-periphery cells and periphery cells surrounding the non-periphery cells (Higuchi: Figure 1 element 100)(The processing elements make up a 2-d array. The processing elements on the outside of the 2-d array make up the periphery cells and the inner four processing elements are the non-periphery cells.);

communicatively connecting the periphery cells to said processor by an interface module having a mechanism for reconfiguring a plurality of information paths between the interface module and respective said periphery cells (Higuchi: Figures 1 and 3 elements 132-139 and 116, column 8 lines 33-40 and column 15 lines 1-7)(The crossbar network connects the periphery cells to the processor and can be reconfigured pathwise by selector and address decoders of the exchange switch.).

Higuchi failed to teach communicatively connecting each of the non-periphery cells only to the processing cells that are immediately neighboring the non-periphery cell.

However, Cloutier disclosed communicatively connecting each of the non-periphery cells only to the processing cells that are immediately neighboring the non-periphery cell (Cloutier: Figure 1 element 104)(The combination uses the bus routing of Cloutier for the non-periphery cells of Higuchi. The bus routing of Cloutier allows for a non-periphery processing element to connect to only the nearest neighbors.).

The bus routing of Higuchi requires a bus for each connection between all processing elements for each row and column. The advantage of the bus routing of Cloutier is that it reduces the number of buses required for sending data between processing elements, which reduces the required chip space to implement the processing array. One of ordinary skill in the art would have been motivated by this advantage to implement the bus routing of Cloutier into the non-periphery processing elements of Higuchi. Thus, it would have been obvious to one of ordinary skill in the art to implement the bus routing scheme of Cloutier in the non-periphery processing elements of Higuchi for the advantage of reduced chip space requirements.

24. As per claim 25:

The additional limitation(s) of claim 25 basically recite the additional limitation(s) of claim 1. Therefore, claim 25 is rejected for the same reason(s) as claim 1.

Response to Arguments

25. The arguments presented by Applicant in the response, received on 4/2/2009 are not considered persuasive.

26. Applicant argues “Applicant and Applicant's counsel respectfully appreciate the Examiner's courtesy in granting the personal interview held April 1, 2009. At the conclusion of the interview agreement was reached that all of the pending claims, as amended above, overcome all rejections set forth by the Office Action of January 6, 2009."

This argument is not found to be persuasive for the following reason.

Upon taking a closer look at the amendments to claim 1, the examiner has found that Higuchi still reads upon the claimed limitations for the reasons detailed in the rejection. The examiner notes that a specific amendment can overcome the Higuchi reference for claim 1. The examiner rejects the claim by stating that the inner 4 processing elements is the 2-d processing array, with the outside buses and exchanges reading on the interface module. The elements that read upon the border cells are indirectly connected through a crossbar bus and an exchange to send data to one of the inner four processing elements. In figure 2 of the applicants drawings, it's shown that there are the same number of border cell buffers to the number of periphery processing cells and that the border cells are directly connected to the periphery processing cells. These two facts are not shown by Higuchi. Higuchi shows that there are 12 border cells to the four inner processing elements and that the 12 border cells are indirectly connected through the crossbar bus and exchange to connect to one of the inner four processing elements. Thus, an amendment detailing the an equal number of border cells and periphery cells, as well as direct connections between them would overcome the Higuchi reference.

Looking at claims 13 and 20, the proposed amendments to the claims discussed in the interview on April 1, 2009 are substantially missing in the amendment and the claims are still rejected by Higuchi.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

Jacob Petranek
Examiner, Art Unit 2183